SYS TEC ELECTRONIC

ECUcore-5484

Hardware Manual

PCB Version: 4152.3 (PLD) / 4244.0 (FPGA)

Edition November 2009

Status / Changes

Status: released

Date/ Version	Section	Change	Editor
L-1177e_01		initial version	K.Otto
L-1177e_02		FPGA functionality added	K.Otto

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Index of figures and tables

1 Introduction

This manual describes the function and technical data for the ECUcore-5484, but not for the microcontroller Freescale Coldfire MCF5484 or any other supplemental products. Please refer to the corresponding manuals and documentation for any other products you may use.

Low-active signals are denoted by a „/“ in front of the signal name (i.e. “/RD”). The representation “0” indicates a logical-zero or low-level signal. A “1” is the synonym for a logical one or high-level signal.

2 Ordering Information and Support

Part Number	Version
4001000	ECUcore-5484, PLD version
4001013	ECUcore-5484, FPGA ECP2-6
4001015	ECUcore-5484, FPGA ECP2-20

The ECUcore-5484 standard version (batch module) features:

- Freescale MCF5484 MCU with 200 MHz
- 16MiB FLASH
- 64MiB DDR-SDRAM
- 32kiB EEPROM
- CPLD with 320 macrocells (640LUT's)
  alternatively FPGA with 6000 or 21000 LUT's
- Ethernet PHY
- Real-Time-Clock
- Reset-/Watchdog-IC
- Temperature-Sensor
- single power supply 3,3V (all other voltages are derived onboard)
- ESD Handling Instructions (printed version)

You can order a kit with Module and Developmentboard. The Board will provide you for rapid application development.

It delivers:

- power supply connector 9-24VDC and a external power supply
- some Keys and LED's to test IO-functionality,
- Connectors for all module-interfaces
- USB-Host with 2 Connectors
- Ethernet-Switch to duplicate the second Ethernet-Interface
- Potentiometer with SPI-ADC and a EEPROM to test SPI
- programmable LED-Driver to test I²C
- BDM and JTAG-Interfaces
- Expansion connector for developing user periphery (a simple IO-Expansion board with 24 keys and 21 LED's is also available - Ord.No. 4004004)

Software Support:

- Integrated Development Environment with complete GNU toolchain for M68k architecture
- colilo bootloader (pre-installed)
- Linux
- plc-firmware
- CANopen protocol stack (limited function, obj-code library)
- CANopen Configuration Suite (Evaluation Version)
- CAN-Report CAN-bus monitor (Evaluation Version)
- OD-Builder

3 Properties of the ECUcore-5484

3.1 Overview

The ECUcore-5484 belongs to the SYS TEC's ECUcore family. The ECUcore-5484 integrates all elements of a microcontroller system on a board. Due to the most modern SMD packages and by the multilayer design, the module could be manufactured on minimum size.

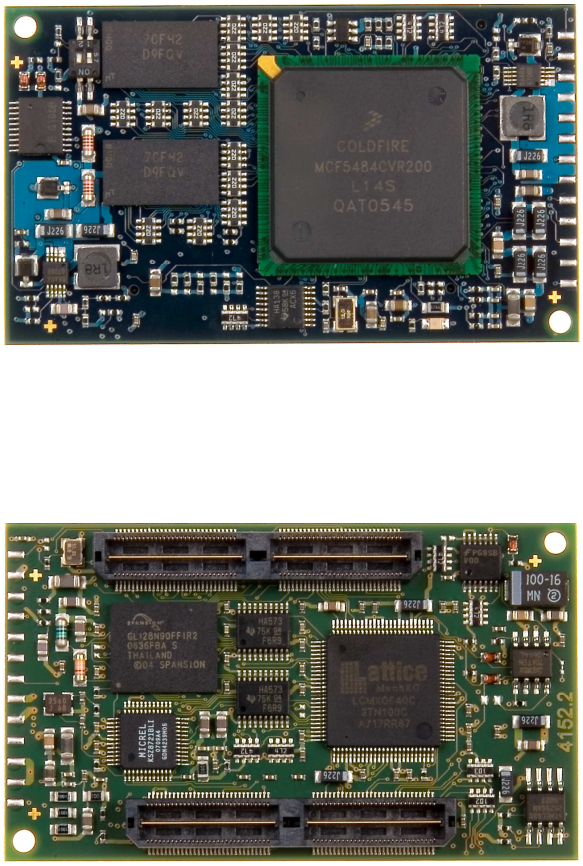

Figure 1: ECUcore-5484

The dimensions of the board are 70mm x 41,5mm and with two included board connectors it is multifunctional in embedded systems.

The ECUcore-5484 includes a Freescale MCF5484 microcontroller. It is a highly-integrated 32-bit microprocessors based on the V4-core of ColdFire microarchitecture.

The interconnection to a baseboard is allowed through a pair of high-density connectors with summary 240 Pin, .

The ECUcore-5484 offers the following features:

- Internal Features of the Freescale Coldfire MCF5484:
    - internal 200MHz CPU-clock from external 33-66,67MHz
    - DDR-/SDR-SDRAM Interface
      32kiB Data- / 32kiB Instruction-Cache
    - 32bit multiplexed address-data bus "Flexbus" for connection of flash and other periphery, usable as 16bit demultiplexed, 6 chip select signals, 33-66MHz,
    - PCI bus (only usable at PLD-version)
    - 32kiB SRAM
    - 2 Fast Ethernet Controller MAC
    - 2 FlexCAN 2.0B controllers, each with 16 message buffers
    - I2C
    - DMA-SPI with 4 (max. 8) chip selects
    - Watchdog Timer
    - 2 Periodic Interrupt Timer
    - 4 General Purpose Timers
    - Interrupt Controller
    - 7 external Interrupts (shared with other functionality)
    - 16-channel DMA
    - GPIO module
    - JTAG/BDM module
    - 388-pin BGA package

- Memory Configuration:
    - 16MiB Flash-Memory (4-64MiB)
    - 64MiB DDR-SDRAM (64-128MiB)
    - 32kiB EEPROM (256Byte – 32kiB)
- Communication features:
    - 4 UART as LVTTL
    - 2 CAN as LVTTL
    - SPI with 8 chip select
    - I²C-Interface
    - 1 Ethernet interface (PHY onboard)
    - 1 Ethernet interface (only MAC)
- Other Board-Level Features:
    - CPLD on Flexbus with 640 LUTs and 34 GPIO's
    - FPGA on Flexbus with 6000 / 21000 LUT's and 80 GPIO's
    - Reset- and Watchdog-IC or Power Sequencer at FPGA version
    - Power failure recognition
    - battery buffered real-time-clock
    - temperature sensor
    - JTAG/BDM module
    - 3.3V operating voltage
      onboad generated core and ddr-sdram-voltages
    - Industrial temperature range (-40°C to +85°C)
    - RoHS compliant

3.2 Block Diagram

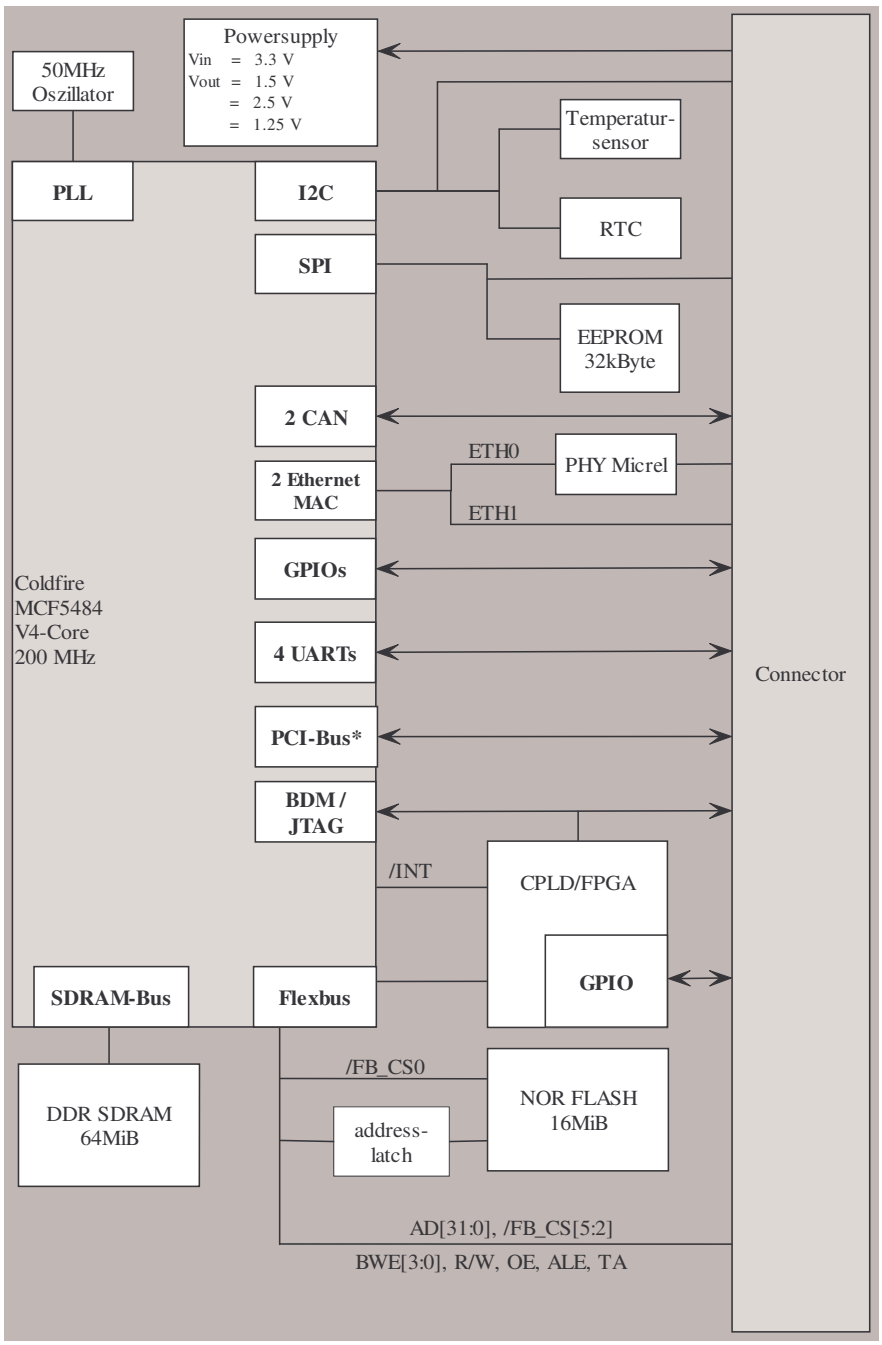

Figure 2: Block Diagram ECUcore-5484

*) CPU-PCI-Bus brought out only at PLD-Version

4 Component Descriptions

The functions of the on-board components are explained in the following sections.

4.1 Pin-header Connection

The ECUcore-5484 has two board connectors. Each of the SMT pin header strips consists of 120 contacts divided into double rows. In total the module has 240 contacts. Separate ground pins in the middle of the connectors provide a large ground connection.
In addition to the high density connectors a on-module BDM/JTAG interface of MCF5484 is prepared by pads at the front of the board.

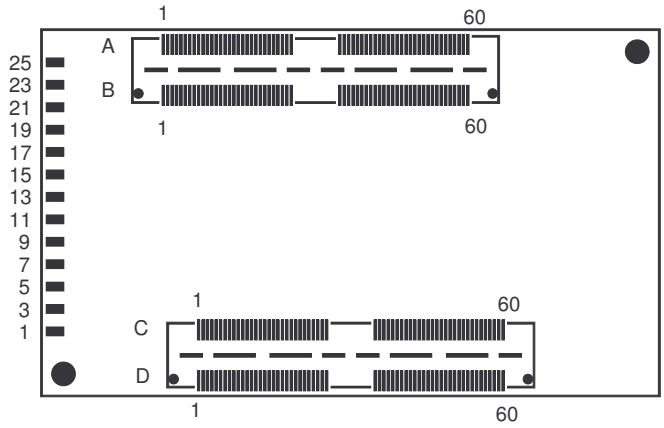

Figure 3: Pinout

The pitch of the board connectors is about 0,5mm. The header connectors equipped on the ECUcore-5484 are the QTH series provided by Samtec.

The series mates with Samtec Products socket series QSH, for example: "QSH-060-01-F-D-A-K". Please refer to the datasheet and their electrical specifications.

The columns A and B representing connector 1. In addition the columns C and D representing connector 2.

The following table defines the pinout.

Signal	Pin	Pin	Signal		Signal	Pin	Pin	Signal
PSTD0	A01	B01	/RSTI		2,5V_EPHY	C01	D01	GND
PSTD1	A02	B02	/MR		GND	C02	D02	Eth0_TX-
PSTD2	A03	B03	/RSTO		Eth0_RX+	C03	D03	Eth0_TX+
PSTD3	A04	B04	/BKPT		Eth0_RX-	C04	D04	GND
PSTD4	A05	B05	PSTCLK		GND	C05	D05	Link/Act
PSTD5	A06	B06	TCK		Speed	C06	D06	PFEC1H0
PSTD6	A07	B07	DSI		PFEC1L0	C07	D07	PFEC1H1
PSTD7	A08	B08	DSO		PFEC1L1	C08	D08	PFEC1H2
SCL	A09	B09	DSCLK		PFEC1L2	C09	D09	PFEC1H3
SDA	A10	B10	MTMOD0		PFEC1L3	C10	D10	PFEC1H4
PCI_0/IO35	A11	B11	PCI_1/IO36		PFEC1L4	C11	D11	PFEC1H5
PCI_2/IO37	A12	B12	PCI_3/IO38		PFEC1L5	C12	D12	PFEC1H6
PCI_4/IO39	A13	B13	PCI_5/IO40		PFEC1L6	C13	D13	PFEC1H7
PCI_6/IO41	A14	B14	PCI_7/IO42		PFEC1L7	C14	D14	E1MDIO
PCI_8/IO43	A15	B15	PCI_9/IO44		CAN_Rx0	C15	D15	E1MDC
PCI_10/IO45	A16	B16	PCI_11/IO46		CAN_Tx0	C16	D16	nc/PWR_TDI
PCI_12/IO47	A17	B17	PCI_13/IO48		CAN_Rx1	C17	D17	nc/PWR_TDO
PCI_14/IO49	A18	B18	PCI_15/IO50		CAN_Tx1	C18	D18	nc/PWR_TMS
PCI_16/IO51	A19	B19	PCI_17/IO52		RxD0	C19	D19	RxD2
PCI_18/IO53	A20	B20	PCI_19/IO54		TxD0	C20	D20	TxD2
PCI_20/IO55	A21	B21	PCI_21/IO56		RxD1	C21	D21	RxD3
PCI_22/IO57	A22	B22	PCI_23/IO58		TxD1	C22	D22	TxD3
PCI_24/IO59	A23	B23	PCI_25/IO60		/PSC1_RTS	C23	D23	/PSC3_RTS
PCI_26/IO61	A24	B24	PCI_27/IO62		/PSC1_CTS	C24	D24	/PSC3_CTS
PCI_28/IO63	A25	B25	PCI_29/IO64		SPI_MTSR	C25	D25	SPI_CLK
PCI_30/IO65	A26	B26	PCI_31/IO66		SPI_MRST	C26	D26	/SPI_CS1
PCI_TRDY/IO67	A27	B27	/PCI_IRDY/IO68		/SPI_CS2	C27	D27	/SPI_CS3
/PCI_CXBE0/IO69	A28	B28	PCI_PAR/IO70		/SPI_CS4	C28	D28	/SPI_CS5
/PCI_CXBE1/IO71	A29	B29	/PCI_PERR/IO72		/SPI_CS6	C29	D29	/SPI_CS7
/PCI_CXBE2/IO73	A30	B30	/PCI_SERR/IO74		/FB_BWE0	C30	D30	/FB_BWE1

Signal	Pin	Pin	Signal		Signal	Pin	Pin	Signal
/PCI_CXBE3/IO75	A31	B31	/PCI_DEVSEL/IO76		/FB_BWE2	C31	D31	/FB_BWE3
PCI_IDSEL/IO77	A32	B32	/PCI_FRAME/IO78		/FB_CS2	C32	D32	/FB_CS3
/PCI_STOP/IO79	A33	B33	/PCI_RESET/IO80		/FB_CS4	C33	D33	/FB_CS5
/PCI_BG0	A34	B34	/PCI_BR0		FB_ALE	C34	D34	/DREQ0
/PCI_BG1	A35	B35	/PCI_BR1		/FB_TA	C35	D35	/BOOT
/PCI_BG2	A36	B36	/PCI_BR2		/DACK0	C36	D36	PFI
/PCI_BG3	A37	B37	/PCI_BR3		/IRQ5	C37	D37	/IRQ6
/PCI_BG4	A38	B38	/PCI_BR4		/IRQ7	C38	D38	TIN0
FB_AD0	A39	B39	FB_AD1		TOUT0	C39	D39	TIN1
FB_AD2	A40	B40	FB_AD3		TOUT1	C40	D40	TIN3
FB_AD4	A41	B41	FB_AD5		TOUT3	C41	D41	IO0
FB_AD6	A42	B42	FB_AD7		IO1	C42	D42	IO2
FB_AD8	A43	B43	FB_AD9		IO3	C43	D43	IO4
FB_AD10	A44	B44	FB_AD11		IO5	C44	D44	IO6
FB_AD12	A45	B45	FB_AD13		IO7	C45	D45	IO8
FB_AD14	A46	B46	FB_AD15		IO9	C46	D46	IO10
FB_AD16	A47	B47	FB_AD17		IO11	C47	D47	IO12
FB_AD18	A48	B48	FB_AD19		IO13	C48	D48	IO14
FB_AD20	A49	B49	FB_AD21		IO15	C49	D49	IO16
FB_AD22	A50	B50	FB_AD23		IO17	C50	D50	IO18
FB_AD24	A51	B51	FB_AD25		IO19	C51	D51	IO20
FB_AD26	A52	B52	FB_AD27		IO21	C52	D52	IO22
FB_AD28	A53	B53	FB_AD29		IO23	C53	D53	IO24
FB_AD30	A54	B54	FB_AD31		IO25	C54	D54	IO26
FB_R/W	A55	B55	/FB_OE		IO27	C55	D55	IO28
VBAT	A56	B56	3,3V		IO29	C56	D56	IO30
3,3V	A57	B57	3,3V		IO31	C57	D57	IO32
3,3V	A58	B58	3,3V		IO33	C58	D58	IO34
3,3V	A59	B59	3,3V		PLD_TMS	C59	D59	PLD_TDI
3,3V	A60	B60	3,3V		PLD_TCK	C60	D60	PLD_TDO

Table 1: Pinout high density connectors

When two pin assignments at pin then first is for module with PLD and second for module with FPGA.

The following table shows the BDM/JTAG layout with pin names.

Signal	Pin	Pin	Signal
not connected	1	2	/BKPT
GND	3	4	DSCLK
GND	5	6	TCK
/RSTI	7	8	DSI
3,3V	9	10	DSO
GND	11	12	PSTD7
PSTD6	13	14	PSTD5
PSTD4	15	16	PSTD3
PSTD2	17	18	PSTD1
PSTD0	19	20	GND
not connected	21	22	not connected
GND	23	24	PSTCLK
not connected	25	26	/FB_TA

Table 2: BDM/JTAG module

The following table defines the function of signals. Most modul pins have the same name like the IC-Pin. So you can find in the relevant datasheet additional informations about the functionality.

Signal	Function (alternate function)	Dir	On-board usage (only MCF5484-signals)	Transmitter /Receiver
PSTD0..PSTD7	BDM/JTAG-Interface of MCF5484			MCF5484
/BKPT				
PSTCLK				
TCK				
DSI				
DSO				
DSCLK				
MTMOD0	signal to choose between BDM and JTAG mode	I	pulldown (low = BDM mode)	MCF5484
/RSTI	Reset output of Reset/Watchdog-IC	I/O	Reset input of CPU, Flash, PLD, Eth-PHY	Reset-IC
/MR	Manual Reset input of Reset/Watchdog-IC	I	pullup	Reset-IC
/RSTO	Reset output of MCF5484	O		MCF5484
SCL	I²C interface	I/O	Temperature sensor, RTC	MCF5484
SDA		I/O		
PCI_0..AD31	PCI-Bus			MCF5484
PCI_TRDY				
/PCI_IRDY				
PCI_PAR				
/PCI_PERR				
/PCI_SERR				
/PCI_CXBE0..3				
/PCI_DEVSEL				
/PCI_FRAME				

Signal	Function (alternate function)	Dir	On-board usage (only MCF5484-signals)	Transmitter /Receiver
PCI_IDSEL				
/PCI_STOP				
/PCI_RESET				
/PCI_BG0..4	PCI-Bus / GPIO	I/O		MCF5484
/PCI_BR0..4	PCI-Bus / GPIO	I/O	/PCI_BR4 is default used as /INT-signal from PLD to CPU	MCF5484
FB_AD0..AD31	Flexbus address/data	I/O	Flash, PLD	MCF5484
FB_R/W	Flexbus read/write	O		
/FB_OE	Flexbus output enable	O		
FB_ALE	Flexbus address latch enable	O		
/FB_BWE0..3	Flexbus byte write enable	O		
/FB_CS2..5	Flexbus chip select	O		
/FB_TA	Flexbus transfer acknowledge	I		
Eth0_TX+, TX-	Ethernet interface0 (PHY)	O		Ethernet PHY Micrel KS8721BL
Eth0_RX+, RX-		I		
2,5V_EPHY	Common voltage of interface0	O		
Link/Act "LED0"	Link/Act Indicator interface 0	O	onboard LED	
Speed "LED1"	Speed Indicator interface 0	O		
PFEC1L0..7 PFEC1H0..7	Ethernet Interface 1 (MAC) MII- or 7Wire-Interface / GPIO	IO		MCF5484
E1MDIO	Ethernet Interface 1	I/O		
E1MDC	Ethernet Interface 1	O		
nc	no function (faulty USB Device interface)	I/O		MCF5484
CAN_Rx0, Rx1	CAN-Interface LVTTL-Level	I		MCF5484
CAN_Tx0, Tx1		O		
RxD0..3	UART0..3 LVTTL-Level	I		MCF5484
TxD0..3		O		
/PSC1_RTS	handshake signals of UART1 / GPIO	I/O		MCF5484
/PSC1_CTS			onboard pullup 4,7k and Switch 1-1 to GND	
/PSC3_RTS	handshake signals of UART3 / GPIO			
/PSC3_CTS				
SPI_MTSR	DSPI interface	I/O		MCF5484
SPI_MRST				
SPI_CLK				
/SPI1..7		O		/CS demux ICr
/BOOT	signal on /DACK1 to determine the boot-sequence (to colilo or Linux)	I	pullup (4,7k) and switch (S1-2) to GND	MCF5484
/PFI	power fail input of reset-ic		pullup 4,7k to 3,3V	Reset-IC
/DREQ0, /DACK0	DMA controller / GPIO	I/O		

Signal	Function (alternate function)	Dir	On-board usage (only MCF5484-signals)	Transmitter /Receiver
/IRQ7	Interrupt input (NMI)	I	pullup 4,7k	MCF5484
/IRQ6, 5	Interrupt input / GPIO	I/O		
TIN0..1	Timer input	I		MCF5484
TIN2..3	Timer input / GPIO	I/O		
TOUT0..1	Timer output	O		
TOUT2..3	Timer output / GPIO	I/O		
IO0..80	GPIO (depends on pld-configuration)	I/O		PLD
PLD_TMS	PLD JTAG interface			
PLD_TCK				
PLD_TDI				
PLD_TDO				
PWR_TMS	PowerSequencer JTAG interface			
PWR_TDI				
PWR_TDO				
VBAT	Buffer supply for RTC (3,3V)	I		RTC
3,3V	power supply of module	I		

Table 3: Signal description

4.2 Jumper Configuration

On default the jumpers are configuered for a prperly function of module. Change positions only if you really need it in a special application ! Read user manual of MCF5484 for the boot and reset-configuration before you change the configuration jumpers J1-J6 !
The following figure shows the positions of jumpers. All placed on top-side of module.

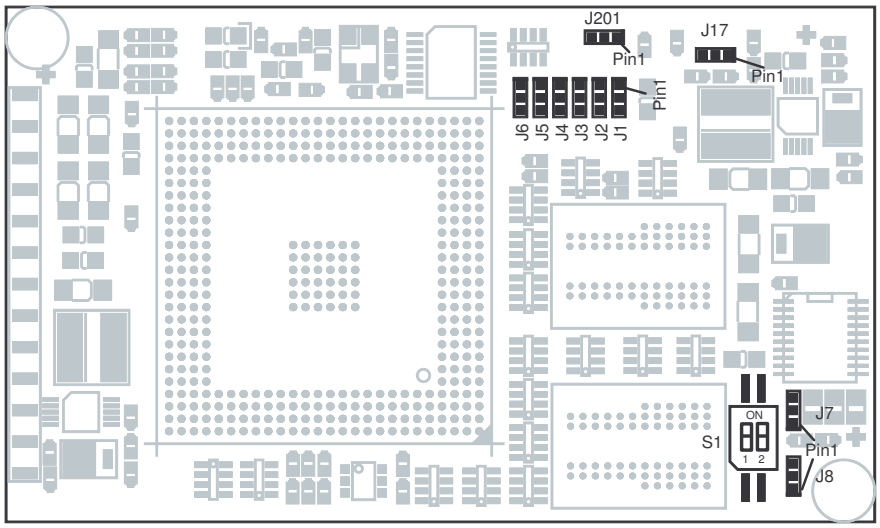

Figure 4: Jumper positions PCB 4152.3 (PLD)

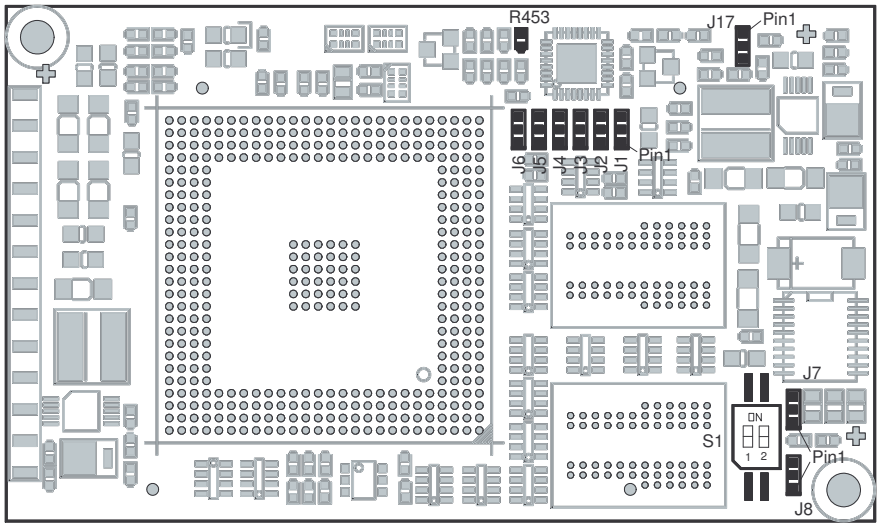

Figure 5: Jumper positions PCB 4244.0 (FPGA)

The function of S1 depence on application. Read the manual of software for further informations.
The following table lists each solder jumper and its function on the ECUcore-5484.

Jumper	Jumper Pad Setting	Signal	Function
J1	2-3 (default)	FB_AD2	FB_CS0 enable autoacknowledge
	1-2		disable
J2	2-3 (default)	FB_AD3	BWE/BE configured as /BWE
	1-2		BWE/BE configured as /BE
J3	1-2 default	FB_AD5	BWE/BE3..0 used as BWE/BE
	2-3		BWE/BE3..2 used as TSIZ1..0 BWE/BE1..0 used as FB_AD1..0
J4/J5/J6	2-3/1-2/1-2 (default)	FB_AD9/10/11	together with AD8=1 and AD12=0 FB_AD12..8 = 00011 = ext.50MHz , int. 100MHz, core 200MHz
	other		not possible with the oscillator
J7/J8	1-2/1-2 (default)	/PSC1_CTS	S1-1 switches /PSC1_CTS (onboard pullup) to GND
	2-3/2-3	MTMOD0	S1-1 switches MTMOD0 (onboard pulldown) to 3,3V
J17	2-3 default	EEPROM-/WP	read/write operations are possible
	1-2		depence on WPEN-Bit write operations are inhibited
J201 (PLD module only)	1-2 (default)	PLD_IRQ	/IRQ-signal of PLD is connected to /PCI_BR4 (=/INT4 of CPU)
	2-3		connected to TIN3 (=/INT3 of CPU)

Table 4: Overview of the Solder Jumpers and Default Settings

4.3 Power Supply

The ECUcore-5484 must be supplied with an input voltage of +3.3VDC. The typical current consumption is approximately 600mA.

The 3,3V supplys directly:

- MCF5484 IO voltage
- CPLD/FPGA
- Flash
- RTC, Temperaturesensor, EEPROM
- Logic

So be carefully and provide a good voltage with low tolerance and low ripple. See "Technical Data" for detailed informations.
The rise time of power on ramp of 3,3V should be slower than 1µs (for MCF5484) and faster than 30ms (CPLD-requirement).

The onboard switching regulators generate all the other needed voltages. These are:

- 1,5V for MCF5484 core, core-pll, usb-pll supply
- 2,5V for DDR-SDRAM supply
- 1,25V for DDR-SDRAM reference
- 1,2V for FPGA Core supply

A Reset-IC watches the voltages 2,5V and 1,5V and reset's the board if one voltage dropes below 0,7V. The 3,3V will be watched too, and a reset is occured if this voltage dropes below 3,08V.

For FPGA a PowerSequencer is needed. It watch all voltages and realized the power on sequence for FPGA. Other functions are reset, watchdog and power fail function.

4.4 Reset Characteristics

Basically the reset characteristics are defined by the EXAR Supervisory Circuit SP706T, which is responsible for generating the system reset signal /RSTI. For FPGA-version the functionality of reset-ic is implemented in power-sequencer.

The reset in signal (/RSTI) is low-active and connected to a pull-up resistor. It is asserted by the following parameters:

- Power Supply Voltage V_{CC} drops below 3.08V
- Manual Reset (/MR) voltage drops below 0.6V
- WDI pin: no signal shift occurs within a timespan of 1.6s

An internal timer releases /RESET after 200ms. When a brownout condition occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. As soon as reset is released and WDI is driven HIGH or LOW, the timer will start counting. Pulses with a minimum pulse width of 50ns can be detected.

The Reset-IC has a build in watchdog timer. During reset the watchdog timer will stay cleared and will not count. It will started when the coldfire-pin /PSC0_RTS (used as watchdog trigger) left the tristate-state and drives a high or low. Then this pin must toggle into 1,6sec. to trigger the watchdog. The output is coupled with /RSTI by Diodes.

The Power Fail Input signal (PFI) is connected to PFI-input of Reset-IC with an 4,7k pullup. It can be switched externaly by open-collector or LVTTL output. The detection of power fail should be near the power supply input of the device (e.g. the 24VDC supply). So you can use a longer time to save critical data or send messages about the error.
To connect the signal /PFO of Reset-IC to external interrupt /INT6 close the soldering jumper R408 (R453 on FPGA version) with 0R. Default the Resistor is open and the /INT6 can used as GPIO or for other interrupt sources. You can find the resistor-pads at Pin 5 of SP706T on the bottom side of module.

4.5 Chip Configuration after Reset

The Chip Configuration will be read on Flexbus-pins at reset FB_AD12..FB_AD0. Don't drive this signale by external IC's during the reset-state. Generaly make shure that the bus devices only drives if her chip-select is activated by Coldfire.

See Chapter "Jumper Configuration" Table "Overview of the Solder Jumpers and Default Settings" for default configuration. Jumpers are mounted with 4,7k-Resistors.

The configuration is chose to support the onboard Flash and PLD with following features:

- portsize for /CS0 (Flash) is 16Bit
- autoacknowledge for /CS0 is enabled
- BWE3..0 of /CS0 is only asserted for write cycles
- Flexbus is used for both address and data
  (PCIbus can completely used separate)
- /BE/BWE3..0 is used as byte/byte write enable
- clock ratio is configured for external 50MHz oszillator, internal 100MHz clock and core 200 MHz clock

4.6 Memory Interface

The external memory interface of the MCF-5484 is divided into external SDRAM and Flexbus. For data storage a eeprom is used connected to SPI-bus.

External SDRAM and Flexbus are 2 separate bus-systems with different portpins on MCF5484. Flexbus is used onboard for Flash and PLD an accessible on board-connector. SDRAM-bus is only used onboard.

4.6.1 SDRAM-Bus

The SDRAM-bus supports SDR-SDRAM and DDR-SDRAM. Onboard two 16bit DDR-SDRAM's mounted, accessible as one 32bit-device. Addressing is realized with /SD_CS0. Default RAM-Types are "Micron MT46V16M16BG-75" or compatible with 32MiB each and 7,5ns cycle time.

4.6.2 Flexbus

Flash-Memory:
Flexbus is connected to Flash via address latch for demultiplexed address bus. One Flash-IC with 16bit data-bus is mounted.
Default Flash-Type is "Spansion S29GL128N10" with 16MiB and 100ns cycle time.
Used Flexbus control signals: /FB_CS0, /FB_OE, FB_R/W, FB_ALE

PLD/FPGA:
For fast accessing the PLD the flexbus is using too. The complete address/data bus pins of MCF5484 are connected to PLD. Demultiplexing can be effect in PLD.
Used Flexbus control signals: /FB_CS1, /FB_OE, FB_R/W, FB_ALE

4.7 Ethernet Controller

The MCF5484 supports two 10/100 Ethernet channels by internal MAC with MII-interface.
For the first channel a on-board PHY chip KSZ8721BLI from Micrel realized a 10/100 physical interface.
Board connector signals are:

Signal	description
Eth0_Tx+	Tx+ from PHY
Eth0_Tx-	Tx- from PHY
Eth0_Rx+	Rx+ from PHY
Eth0_Rx-	Rx- from PHY
2V5_EPHY	2,5V PHY-Supply
Link/Act	output for LED (parallel a yellow LED is mounted on board with 270R)
Speed	output for LED

Tx and Rx Signals are pulled up with 49,9R to 2,5V-EPHY.

The second MII-interface is brought out to board connector.

The MII-Interfaces defaults to GPIO after reset. The GPIO module must be configured to enable the peripheral function of the appropriate pins prior to configuring the Fast Ethernet Controller.

4.7.1 MAC Address

SYS TEC electronic has aquired a pool of these MAC addresses. The MAC address for the first Ethernet-Interface Eth0 is barcode-labelled attached on the ECUcore-5484.

4.8 I2C-Module

The ECUcore-5484 features one I2C interface, a 2-wire serial bus used for communication with I2C devices. The bus is brought out via the board connector. The ECUcore-5484 comes with two on-board I2C devices. Please refer to the table below.

I2C device	Address
Real-Time-Clock Epson 8564JE (U201)	0xA2
Temperature Sensor TI TMP101 (U202)	0x90 (default) 0x92 upon request

Table 5: I2C Components

The I2C-Module defaults to GPIO after reset. The GPIO module must be configured to enable the peripheral function of the appropriate pins prior to configuring the I2C-Module.

4.8.1 Real-Time-Clock

The ECUcore-5484 is equipped with a Real-Time-Clock to manage real-time application. The device offers functions such as calendar clock, alarm and timer. It also outputs pre-defined frequencies (32.768kHz, 1024Hz, 32Hz, 1Hz) via the CLKOUT pin.

RTC Characteristics:

- Built-in crystal running at 32768Hz
- programmable alarm, timer and interrupt functions
- low power consumption:
  - Bus active: ≤ 1mA
  - Bus inactive, CLKOUT inactive: ≤ 1µA

The Real-Time-Clock is supplied by 3.3V DC. If the system voltage crashes, the backup battery supplies the RTC (if connected!).

Device Address:

- 0xA2 when write mode
- 0xA3 when read mode

The Pin CLKOE is pulled high. So the clock output can be enabled by setting the bit 'FE' in Register 'Clock Out frequency' to 1.

One of the output-pins of RTC can connect to CPU-pin '/DREQ1_/IRQ1'.

resistor	function (when R equipped)
R15 (default equipped)	CLKOUT is connected to /IRQ1
R16 (default open)	/RTC_INT is connected to /IRQ1

At module with FPGA both signals are connected to FPGA-Pins and can be used in Software.

4.8.2 Temperature Sensor

The ECUcore-5484 disposes of an optional temperature sensor TMP101 to record ambient temperatures to, e.g, enable protection from overheating. The ECUcore-5484 just provides the physical connection between the CPU and the sensor. The communication or any protective measures are software functions to be provided by the user application.

The address is adjustable by a resisitor. The following table shows the various assembly options.

resistor	ADD0 signal	Address
equipped (default)	0 (GND)	1001000x = 0x90
not equipped (upon request)	float	1001001x = 0x92

Table 6: Temperature Sensor Address

Temperature sensor characteristics:

- Temperature resolution of 0.0625°C
- Temperature range of -55°C to +125°C
- Alert pin as interrupt source if temperature exceeds defined limits

The Alert-Pin is connected to CPU-Pin '/PSC0_CTS' and must be polled to indicate temperature-exceedings.

4.9 DSPI-Interface

The ECUcore-5484 allows high-speed serial communication with SPI devices such as EEPROM. The DSPI bus signals are brought out via the board connector.

An onboard 3-to-8 decoder provides up to 8 SPI chip select signals of which one is reserved for use with EEPROM and 7 are available via the board connector.

Addressed-decoding:

DSPI_CS pins of CPU				decoder chipselect
CS0	CS2	CS3	CS5	low activ
0	0	0	1	no chip select
0	0	0	0	/CS-EEPROM
1	0	0	0	/SPI_CS1
0	1	0	0	/SPI_CS2
1	1	0	0	/SPI_CS3
0	0	1	0	/SPI_CS4
1	0	1	0	/SPI_CS5
1	1	0	0	/SPI_CS6
1	1	1	0	/SPI_CS7

The following table shows the SPI signals available.

SPI signal (on CPU)	**Description**
/SPI_CS1-7	Chip Select's on connector
SPI_MTSR (SOUT)	Master Transmit Slave Receive
SPI_MRST (SIN)	Master Receive Slave Transmit
SPI_CLK (SCK)	Clock

Table 7: SPI Signals

The DSPI module defaults to GPIO after reset. The GPIO module must be configured to enable the peripheral function of the appropriate pins prior to configuring the DSPI module.

4.9.1 EEPROM

The ECUcore-5484 has an EEPROM for data storage. In standard version the EEPROM provides 32kiB (Typ ATMEL AT25256A). The following table shows the pinout connection.

Signal EEPROM	Signal MCF5484	Description
SO	PSPI_MRST	Serial Output EEPROM
SI	PSPI_MTSR	Serial Input EEPROM
SCK	PSPI_CLK	Clock EEPROM
/CS	PSPI_/CS0	Chip Select EEPROM
/WP	Jumper J17	Write Protect EEPROM for data protection 1: normal read/write (default) 0: write protect is active
/HOLD	N.C.	connected to high, Suspends Serial Input, is not supported

Table 8: EEPROM Signals

4.9.2 CAN Interface

The MCF5484 includes 2 CAN interfaces. The 2 channels are brought out via the board connector as LVTTL-interface. The CPU provides different Pins for CAN. The default connection is:

CAN-Signal	Pin MCF5484	Connector-Pin
CANRX0	/PSC2CTS	CAN_Rx0 (X400/C15)
CANTX0	/PSC2RTS	CAN_Tx0 (X400/C16)
CANRX1	TIN2	CAN_Rx1 (C400/C17)
CANTX1	TOUT2	CAN_Tx1 (X400/C18)

Table 9: CAN Signals

Externaly an 3,3V CAN-Transceiver can directly connected to CAN-Pins. Alternatively a galvanic decoupled CAN-Interface can build to save the module. Drive Capability of CAN output pins is 8mA.

4.10 Serial Interface

The ECUcore-5484 supports up to 4 independent UARTs available on the board connector. They are used to interface serial communication via RS232 or RS485 level signals. Each interface has two handshake-signals (RTS/CTS), but not all are supported on module. The following table shows the pinout. Signals are LVTTL. However, the board does not provide any transceiver.

Signal MCF5484	Signal Connector	Comment
PSC0TXD	TxD0	
PSC0RXD	RxD0	
/PSC0CTS	N.C.	used as WDI for onboard Watchdog-IC
/PSC0RTS	N.C.	used for Temperature-Sensor INT-Pin
PSC1TXD	TxD1	
PSC1RXD	RxD1	
/PSC1CTS	PSC_IO2	
/PSC1RTS	PSC_IO3	used as second Boot-Signal with pullup (4k7) and DIP-Switch 2 to GND (s.a. Jumper J8)
PSC2TXD	TxD2	
PSC2RXD	RxD2	
/PSC2CTS	CAN_Tx0	when CAN0 not needed this Pins can be used for PSC2-Handshake
/PSC2RTS	CAN_Rx0	
PSC3TXD	TxD3	
PSC3RXD	RxD3	
/PSC3CTS	PSC_IO6	GPIO's can be used for PSC3-Handshake
/PSC3RTS	PSC_IO7	

Table 10: UART Signals

The UART-Modules default to GPIO after reset. The GPIO module must be configured to enable the peripheral function of the appropriate pins prior to configuring the UART module.

4.11 DMA controller

There are two external DMA-Interfaces on MCF5484 consist of DMA-acknowledge-Pin and DMA-request-Pin. Only one interface is provided by module as default.

Signal MCF5484	Signal Connector	comment
/DREQ0	/DREQ0	
/DACK0	/DACK0	
/DREQ1	/IRQ1	default onboard connected to RTC-CLKOUT via 0R-Resistor or to FPGA
/DACK1	/BOOT	onboard connected to Boot-Switch (DIP-Switch 1) with pullup 4k7

Table 11: Timer Signals

To find more informations about DMA as Communication Subsystem see the user manual of MCF5484.

4.12 BDM/JTAG Port of MCF5484

The ECUcore-5484 provides a BDM/JTAG interface for the CPU MCF5484. This is for debugging on low level software and programming the CPU of raw module. In default the module will distributed with a bootloader to download software over ethernet or RS232.

BDM/JTAG is accsessible over board connector.
The ECUcore-5484 has a specific BDM/JTAG pinout on the short side of the board. Here a debug-adapter (e.g. BDM Adapter from P&E-Microcomputer Systems) can directly be plugged. So you can get a debug-module for target environment, without BDM-connectors on baseboard.

The function BDM or JTAG is selectable with Signal MTMOD0 on board-connector or on DIP-SW1 (not default, see description J7/J8).
The MTMOD0-Pin has a 4k7 pulldown on board.

MTMOD0	function
0 (default)	normal and Background Debug Mode (BDM)
1	normal and JTAG mode

Some of the BDM/JTAG Pins has a 4,7k pullup or pulldown resistor on board:

resistor	signal
pullup	/BKPT, DSI, DSO, DSCLK
pulldown	TCK

4.13 CPLD

A second JTAG-Port is brought out on the board connector for programming the CPLD. All Pins has on bord 10k pullup or pulldown resistors.

resistor	signal
pullup	PLD_TDI, PLD_TDO, PLD_TMS
pulldown	PLD_TCK

PLD-JTAG-signals are onboard connect to MCF5484. So Modules with Linux supports programming of CPLD from CPU and don't need external programming devices for PLD.

The Lattice CPLD Type MachXO640 with speed grade '-3' is used.

4.14 FPGA

FPGA is used to provide more functionality. There are more IO-Pin's and Gates in the FPGA for more flexibilty. This make it possible e.g. to realize more than one 32bit counter-inputs and pulse-outputs.
The PCI pins at connector would changed in FPGA-IO-Pins. So there are 80 FPGA-IO's for various functions.

SPI /CS-generation like chapter 4.9 is implemented in FPGA.
SPI-MRST, MTSR and CLK are connected to the FPGA too. So it can be assigned to any othe IO-Pin. Other way is to implement a external SPI-unit in FPGA to release the cpu from SPI-communication.

For faster signal handling the cpu-interrupt-pins IRQ1, 3, 4 and 6 are connected to FPGA.

The Lattice Type "LFE2-6SE-5FN256I" or "LFE2-20SE-6FN256I" are used.
Programming of FPGA is the same like PLD.

5 Technical Data

The physical dimensions of the ECUcore-5484 are shown in the figure below.

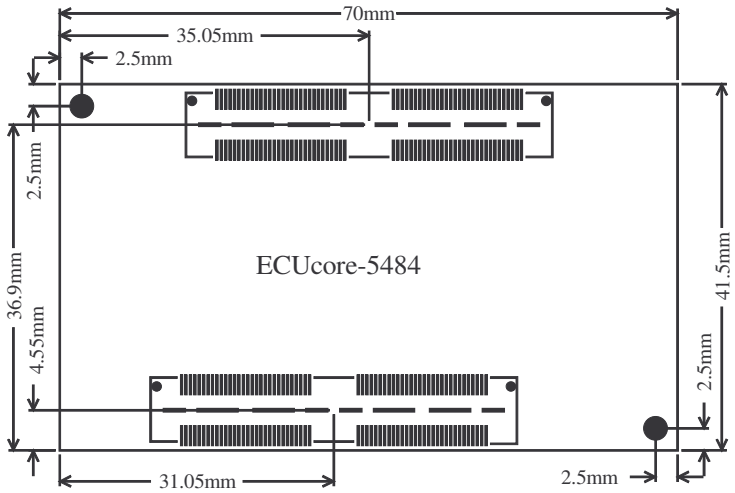

Figure 6: Physical Dimensions

The height including board connector and components is about 9mm. The thickness of the PCB is about 1.6mm. The maximum component height on top is about 2,55mm.

dimensions	70mm x 36,9mm x 7,8mm
weight	approximately 21g
operating temperature	-40°C to +85°C
storage temperature	-40°C to +85°C
operating voltage	+3.3V DC ± 5%
current consumption	typ. 600mA
I/O-Level	+3.3V DC ± 5%

Table 12: Technical Data

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How would you improve this manual?

Did you find any mistakes in this manual? page

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